

U.S.P.N. 10,769,245

Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification has been amended to correct grammatical errors as graciously suggested by Examiner.

The claims have been amended and new claims added to clarify Applicants disclosed and claimed invention.

Support for the amendments and new claims is found in the original claims and the Specification.

No new matter has been added.

For example support for Applicants amended claims is found in the original claims and in the Specification at paragraphs 0034 and 0035;

"The present invention contemplates a new and improved method for the cleaning of wafers and is particularly applicable to the cleaning of wafers during a chemical mechanical polishing (CMP) process. The method includes

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polishing a material layer or layers, particularly a metal layer or a hydrophobic, low-k dielectric layer or layers, on a wafer at sequential polishing steps in a polishing sequence. After at least one of the polishing steps, a novel surfactant composition solution is applied to the polished layer in a surfactant rinse step, followed typically by rinsing of the layer using high-pressure deionized water in a water rinse step.

Preferably, the surfactant composition solution is applied to a polished layer after the last polishing step in the polishing sequence. Most preferably, the surfactant is applied to a polished layer after each polishing step in the polishing sequence. The surfactant composition solution imparts a generally hydrophilic character to the layer, rendering the layer amenable to cleaning by deionized water. This significantly enhances the removal of particles from the layer and substantially reduces the number of CMP-induced defects. Furthermore, the surfactant composition solution stabilizes the polishing rate by cleaning the surface of the polishing pad on the CMP apparatus."

Support for new claims 21 through 30 is found in the Specification including Figure 2.

Claim Rejections under 35 USC 102

1. Claims 1-10, and 13-15 stand rejected under 35 USC 102(b) as

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anticipated by Lu et al. (US 6,361,407).

Lu et al. teach a CMP process for polishing silicon wafers, where the wafer is polished, **then contacted with a surfactant, and then the wafer polishing surface is dried prior to rinsing the polishing surface** and carrying out a final polishing step (see Abstract; Figure 1; Figure 2; col 1, lines 9-24, col 2, lines 21-23; col 2, lines 36-49; col 6, lines 30-55). The process is taught to reduce defects including etching stains.

In another aspect of the method of Lu et al., an acidic quench solution is applied to the wafer prior to applying the surfactant disclosed to preferably be polyoxyethylene glycol (col 2, lines 57-65; col 5, lines 37-40; col 6, lines 1-20)). One object of the invention is **to form a substantially continuous hydrophobic protective layer** on the polished surface of the semiconductor wafer (col 3, lines 4-17) by applying the polyoxyethylene glycol after polishing and then allowing the wafer to dry (col 3, lines 4-17; col 6, lines 55-61; col 7, lines 47-62), **prior to rinsing**. Lu et al. additionally disclose that the surfactant may include C4-C18 alkyl, alkene and aryl groups, preferably straight chain **alkyl or alkene** groups with P as a

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polar substituent selected from the group consisting of OH, COOH, SO₃, SO₄, and NH₂ (see col 5, lines 54-68).

Thus, Lu et al. do not disclose several aspects of Applicants disclosed and claimed invention including:

"providing a wafer surface comprising at least one of a metal and a dielectric layer;

providing a surfactant composition solution;

subjecting said wafer surface to a plurality of polishing steps;

applying said surfactant composition solution to said wafer surface after at least one of said plurality of polishing steps to render said wafer surface hydrophilic; and

then rinsing said wafer surface."

2. Claim 11 stands rejected under 35 USC 102(b) as anticipated by, or in the alternative, under 35 USC 103(a) as obvious over Lu

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et al., above.

Applicants reiterate the comments made above with respect to Lu et al. and note that Lu et al. do not disclose Applicants polishing process or polishing surface, or polishing sequence, but rather teaches a process that works by a different principle of operation, i.e., makes the surface **hydrophobic** by drying a surfactant solution on the wafer surface **prior to rinsing**.

Lu et al. is clearly insufficient to make out a prima facie case of obviousness with respect to Applicants disclosed an claimed invention.

Claim Rejections under 35 USC 103

1. Claims 12 and 16 stand rejected under 35 USC 103(a) as unpatentable over Lu et al., above, in view of WO 03065433 (Ikemoto et al.)

Applicants reiterate the comments made above with respect to Lu et al.

Ikemoto et al. (WO '433) disclose:

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"A liquid detergent for semiconductor device substrates which comprises the following ingredients (A), (B), and (C); and a method of cleaning with the detergent. Ingredient (A): an ethylene oxide type surfactant which comprises a hydrocarbon group optionally having a substituent (excluding phenyl) and a polyoxyethylene group, and in which the ratio of the number of carbon atoms in the hydrocarbon group (m) to that of oxyethylene groups in the polyoxyethylene group (n), m/n , is from 1 to 1.5, the number of the carbon atoms (m) is 9 or larger, and the number of the oxyethylene groups (n) is 7 or larger. Ingredient (B): water. Ingredient (C): an alkali or an organic acid."

Examiner has not pointed to support for his assertion that "ethylene oxide or its derivatives are conventionally utilized in the art as non-ionic surfactants". In addition, as seen above, Ikemoto et al. (WO '433) disclose "an ethylene oxide type surfactant **which comprises a hydrocarbon group optionally having a substituent (excluding phenyl) and a polyoxyethylene group.**"

Ikemoto et al. (WO '433) does not disclose an aqueous alcohol solution or an aqueous alcohol solution including

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ethylene oxide.

There is no apparent motivation to combine the teachings of Lu et al., who teach cleaning a semiconductor wafer (without overlying dielectric or metal layers) by drying a surfactant on the semiconductor wafer surface prior to rinsing, with the teachings of Ikemoto et al. (WO '433), who do not disclose or teach that the composition of Ikemoto et al. (WO '433) could be successfully used to form a dried surfactant on the semiconductor wafer surface to form a hydrophobic surface according to the method of Lu et al.

Nevertheless, even assuming *arguendo* a proper motivation for combination, such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success **must both be found in the prior art, and not based on applicant's disclosure.**" *In re Vaeck*, 947

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F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." *In re Ratti*, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

"we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination" *Symbol Technologies, Inc. v. Opticon, Inc.*, 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).

The cited references, either singly or in combination, fail to make out a *prima facie* case of obviousness with respect to

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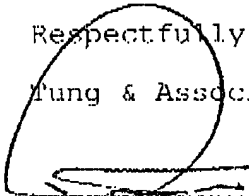
Applicants disclosed and claimed invention.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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